

ABSTRACT OF THE DISCLOSURE

An input/output buffer protection circuit, which comprises an I/O pad, an I/O buffer, an n-well control circuit, a gate control circuit, and a protection component. The I/O buffer 5 includes a PMOS transistor and a NMOS transistor. The n-well control circuit is coupled to an n-well of the PMOS transistor. When an input voltage higher than a source voltage is applied, voltage at the n-well of the PMOS is increased by the n-well control circuit to the input voltage level. The gate control 10 circuit is coupled to the gate terminal of the PMOS transistor and the input/output pad. When an input voltage higher than a source voltage is applied, voltage at the gate terminal of the PMOS is increased by the gate control circuit to the source voltage level. Wherein the gate control circuit comprises a 15 transistor and the transistor transfers a high potential control voltage to the gate of the PMOS transistor in output mode. The protection component is coupled between the gate of the transistor and the I/O pad to generate a voltage drop down path and block the I/O pad signal from flowing back to the gate of 20 the transistor.